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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,311	05/25/2001	Tetsuya Aoyama	503.40146X00	2824

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EXAMINER	
LANEAU, RONALD	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,311	AOYAMA ET AL.	
	Examiner	Art Unit	
	Ronald Laneau	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 15/1-2, 16/1-2, 24/1-2, 25/1-2, 26/1-2, and 27/1-2* is/are rejected.

7)☒ Claim(s) *See Continuation Sheet* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Continuation of Disposition of Claims: Claims objected to are 3, 4, 5-14, 15/3-14, 16/3-14, 17/1-14, 18/3-14, 19/3-14, 22/1-14, 23/22/1-14, 24/3-14, 25/3-14, 26/3-14, and 27/3-14.

DETAILED ACTION

Drawings

1. Figures 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any

inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 2, 15/1-2, 16/1-2, 24/1-2, 25/1-2, 26/1-2, and 27/1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior Art (AAPA) in view of Inamori et al (US 5,751,278).

As per claim 1, the AAPA discloses a conventional display device including a display module 21 provided with a display panel 26 in which pixels of n_{01} pieces in line direction and of n_{0r} pieces in row direction are arranged in a matrix shape (block unit) and displays a picture image at a drive frequency of f_H which gives a pattern for each block, a display control unit 22 which controls the display module 21 and a picture image signal generation unit 24 which generates picture image signals (see AAPA). The AAPA discloses all elements of the claimed invention except a computing circuit inside a display controller as seen in figure 6 but Inamori et al teach a liquid crystal display 102, a display controller 107 wherein a

calculation section 108 (computing circuit) in synchronization with a clock generating circuit that would provide frequencies for the picture image signals for the matrix (block unit) (see fig. 1).

It would have been to one of ordinary skill in the art to utilize the calculation section (computing circuit) taught by Inamori et al into the teaching disclosed in Applicant's Admitted Prior Art (AAPA) as claimed because it would provide a driving device for a display device capable of executing a calculation operation at a high speed (col. 6, lines 28-31).

As per claim 2, the AAPA discloses a display module that is capable of adding Np pieces of the specific patterns (see AAPA). The AAPA does not disclose a computing circuit but Inamori et al teach a display controller a liquid crystal display wherein a calculation section (computing circuit) in synchronization with a clock generating circuit that would provide frequencies for the picture image signals for the matrix (block unit) (see fig. 1).

It would have been obvious to one of ordinary skill in the art to utilize the teachings of Inamori into the AAPA for the same reasons given in claim 1.

As per claim 15/1-2, the AAPA discloses a display device wherein the number of pixels in line direction in a block unit is larger than the number of pixels in row direction in the block unit as claimed (see fig. 3).

As per claim 16/1-2, the AAPA discloses a display device wherein a combination of a plurality of pixels which constitute a block unit is varied as claimed (see fig. 3).

As per claim 24/1-2 and 26/1-2, the AAPA does not disclose that the picture image signal generation unit and the display module include the computing circuit but the combination of the teachings disclosed in the AAPA with the calculation section (computing circuit) taught by Inamori et al would provide a picture image signal generation circuit and a display module including a calculation section (computing circuit) as claimed (see fig. 1, 108).

As per claim 25/1-2, Inamori et al teach a display controller 107 that includes a calculation section 108 (computing circuit) as claimed (see fig. 1).

As per claim 27/1-2, the display module disclosed in the AAPA is an LC display module as claimed (see AAPA).

Allowable Subject Matter

5. Claims 3, 4, 5-14, 15/3-14, 16/3-14, 17/1-14, 18/3-14, 19/3-14, 22/1-14, 23/22/1-14, 24/3-14, 25/3-14, 26/3-14, and 27/3-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

As per claims 3, 15/3, 16/3, 17/3, 18/3, 19/3, 20/19/3, 21/20/19/3, 22/3, 23/22/3, 24/3, 25/3, 26/3, and 27/3, a display device comprising a compression rate regulation unit which modifies the number of pieces Np of the specific patterns.

As per claims 4, 15/4, 16/4, 17/4, 18/4, 19/4, 20/19/4, 21/20/19/4, 22/4, 23/22/4, 24/4, 25/4/ 26/4, and 27/4, a display device comprising a high compression rate computing circuit which modifies the number of the specific patterns to be added for every block unit.

As per claims 5-8, 15/5-8, 16/5-8, 17/5-8, 18/5-8, 19/5-8, 22/5-8, 23/22/5-8, 24/5-8, 25-5-8, 26/5-8, and 27/5-8, a display device wherein the display module includes a panel in which the pixels are arranged in a matrix shape, a signal driver, a scan driver and opposing signal driver, scan lines connected to the scan driver, and opposing signal lines connected to the opposing signal driver; each of the pixels includes a signal electrode, opposing signal electrode, opposing signal electrode and a switch element, the signal electrode is connected to one of the signal lines via the switch element, the opposing signal lines, a first potential is applied to the signal electrodes provided for the pixels on a same line included in a same block unit, a second potential is applied to the opposing signal electrodes

provided for the pixels on a same row included in the same block unit, a certain specific pattern is formed by the first and second potentials for the same block unit concerned and one of the common opposing signal lines is connected to the opposing signal electrodes provided for the pixels on the same line.

As per claims 9-14, 15/9-14, 16/9-14, 17/9-14, 18/9-14, 19/9-14, 22/9-14, 23/22/9-14, 24/914, 25/914, 26/9-14, and 27/9-14, a display device wherein the display module includes a panel in which the pixels are arranged in a matrix shape, a signal driver, a scan driver and opposing signal driver, scan lines connected to the scan driver, and opposing signal lines connected to the opposing signal driver; scan lines connected to the scan driver, opposing signal common lines connected to the opposing signal driver and opposing signal lines connected to the opposing signal common lines; each of the pixels includes a signal electrode, opposing signal electrode and a switch element, the signal electrode is connected to one of the signal lines via the switch element, the opposing signal electrode is connected to one of the opposing signal lines, a first potential is applied to the signal electrodes provided for the pixels on a same line applied in a same block unit, a second potential is applied to the opposing signal electrodes provided for the pixels on a same row included in the same block unit, a certain specific pattern is formed by the first and second potentials for the same block unit concerned and one of

different opposing signal lines is connected to the opposing signal electrodes provided for the pixels included in a different block unit.

As per claim 17/1-2, a display device wherein the display module is a projection type display, and the projection type display includes a projection pattern display source which displays the specific patterns and a pattern display element, and the pattern display element includes a pair of substrates on which a transparent electrode is formed, a photo conductive layer formed on the transparent electrode and an LC layer sandwiched by the pair of substrates.

As per claims 20 and 21, a display device wherein the display module includes a panel in which the pixels are arranged in a matrix shape, a signal driver, a scan driver and a common electrode driver, signal lines connected to the signal driver; scan lines connected to the scan driver; and common electrode lines connected to the common electrode driver, each of the pixels is provided with an adder-subtractor for adding the specific patterns, and the signal lines of which number is equal to the number Np of specific patterns to be added are connected to the adder-subtractor.

As per claim 22/1-2, a display device wherein each circuit which constitutes each pixel includes a sample hold means for digital signal and another sample hold means for analog signals.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Imamura (US 6,466,192) teaches a matrix-type display control device suited for large capacity display, a module controller of a simple matrix-type comprising a low frequency, a timing signal generator, ...
- Ode et al (US 2001/0024183) teach a liquid crystal display device including a liquid crystal panel having a plurality of pixels, a driving circuit applying a video signal voltage to each of the pixels in accordance with display data.
- Ishii et al (US 4,779,083) teach a display control system, a liquid crystal display module, a display controller and a CPU.
- Ode et al (US 6,232,941) teach a liquid crystal display device capable of generating gradation voltages for multilevel gradation, such as 256-level gradation, without increasing the chip size of video signal line driving means.
- Kudo et al (US 2002/0130881) teach a liquid crystal display control having a plurality of pixels, and a controller which selects a pattern corresponding to a gradation of gradation data.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald Laneau whose telephone number is 703-305-3973. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6.00 PM or via email: ronald.laneau@uspto.gov.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached at 703-305-4709.

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Ronald Laneau
Examiner
Art Unit 2674

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December 12, 2002